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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,453	10/29/2003	Ippei Fujimoto	T36-159874M/KOH	4570

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/695,453	FUJIMOTO ET AL.
	Examiner	Art Unit
	Alexander O Williams	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) *4-6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/9/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/695453 Attorney's Docket #: T36-159874M/RS
Filing Date: 10/29/03; claimed foreign priority to 10/31/02

Applicant: Fujimoto et al.

Examiner: Alexander Williams

Applicant's election of Group I (claims 1 to 3), filed 7/22/04, has been acknowledged.

This application contains claims 4 to 6 drawn to an invention non-elected without traverse.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the electrode for p-type Group III nitride compound semiconductor, comprising a film at least containing polycrystalline metal, wherein said polycrystalline metal has such a fiber structure that crystal planes of crystal grains are oriented and wherein said polycrystalline metal has large crystal grains in claims 1-3, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The incorporation of essential material in the specification by reference to a foreign application or patent, or to a publication is improper. Applicant is required to amend the disclosure to include the material incorporated by reference. The amendment must be accompanied by an affidavit or declaration executed by the applicant, or a practitioner representing the applicant, stating that the amendatory material consists of the same material incorporated by reference in the referencing application. See *In re Hawkins*, 486 F.2d 569, 179 USPQ 157 (CCPA 1973); *In re*

Hawkins, 486 F.2d 579, 179 USPQ 163 (CCPA 1973); and *In re Hawkins*, 486 F.2d 577, 179 USPQ 167 (CCPA 1973).

The drawings are objected to under 37 CFR 1.83(b) because they are incomplete. 37 CFR 1.83(b) reads as follows:

> When the invention consists of an improvement on an old machine the drawing must when possible exhibit, in one or more views, the improved portion itself, disconnected from the old structure, and also in another view, so much only of the old structure as will suffice to show the connection of the invention therewith.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to because in the specification, the tables should be included in the drawing.

Correction is required.

Claims 1 to 3 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, it is unclear and confusing to what is meant and what shows "An electrode for p-type Group III nitride compound semiconductor, comprising a film at least containing polycrystalline metal." Where is this structure shown in the drawing?

In claim 2, it is unclear and confusing to what is meant and what shows "said polycrystalline metal has such a fiber structure that crystal planes of crystal grains are oriented." Where is this structure shown in the drawings?

In claim 3, it is unclear and confusing to what is meant and what shows "said polycrystalline metal has large crystal grains." Where is this structure shown in the drawings?

Any of claims 1 to 3 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 3, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Yamanaka (U.S. Patent Application # 2003/0013280 A1).

1. Yamanaka (figures 1 to 59) specifically figure 4(12) show an electrode **15** for p-type Group III nitride compound semiconductor, comprising a film at least containing polycrystalline metal (the phosphorus-doped polycrystalline silicon film 15 used for a gate electrode).

[0086] In the present invention, the low-crystallization semiconductor thin-film may be formed by vapor-phase growth such as catalytic CVD, plasma CVD, or the like, and as a source gas used therefor, for example, there may be mentioned silicon hydride or a derivative thereof; a mixture of silicon hydride or a derivative thereof and a gas containing hydrogen, nitrogen, germanium, carbon, or tin; a mixture of silicon hydride or a derivative thereof and a gas which contains a dopant including a Group III or a Group V element of the periodic table; and a mixture of silicon hydride or a derivative thereof, a gas containing hydrogen, nitrogen, germanium, carbon, or tin, and a dopant including a Group III or a Group V element of the periodic table.

[0407] Next, as shown in FIG. 2(5), in order to optimize the threshold value V.sub.th) by dopant concentration control in the channel region of the p-type MOSTFT, the n-type MOSTFT portions are masked with a photoresist 12 in this case, and n-type dopant ions (such as phosphorus ions) 13 are doped at a dose rate of, for example, 1.times.10.sup.12 atoms/cm.sup.2 by ion implantation or ion doping so as to have a donor concentration of 2.times.10.sup.17 atoms/cc, thereby forming an n-conductive type polycrystalline silicon thin-film 14 from the polycrystalline silicon thin-film 7.

[0408] Subsequently, as shown in FIG. 3(6), after a silicon oxide film (50 nm thick) 8 is formed for a gate insulating film by catalytic CVD or the like, a phosphorus-doped polycrystalline silicon film 15 used for a gate electrode material is formed by catalytic CVD, which is the same method as described above, with supply of 2 to 20 sccm of PH.sub.3 and 20 sccm of SiH.sub.4 so as to have a thickness of, for example, 400 nm.

2. An electrode for p-type Group III nitride compound semiconductor according to claim 1, Yamanaka show wherein said polycrystalline metal has such a fiber structure that crystal planes of crystal grains are oriented.

[0193] In the case described above, since the thermal dissipation is more effectively performed at the linearly projecting portions than the other parts,and conditions (formation of species or nuclei), which may start recrystallization, are prepared thereby, the entire low-crystallization semiconductor thin-film may be converted into a polycrystalline semiconductor thin-film having a large grain size or a single crystalline semiconductor thin-film, each having an optional crystal orientation.

3. An electrode for p-type Group III nitride compound semiconductor according to claim 2, Yamanaka show wherein said polycrystalline metal has large crystal grains.

[0678] In this case, since heat dissipation at the projecting portion 301 is more efficiently performed than that at the other portions, and conditions (formation of species or nuclei), which may start recrystallization, are prepared thereby, the entire low-crystallization semiconductor thin-film may be converted into the polycrystalline semiconductor thin-film having a large grain size or the single crystalline semiconductor thin-film 7, each having an optional crystal orientation.

Claims 1 to 3, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Washio et al. (U.S.Patent # 6,600,178 B1).

1. An electrode for p-type Group III nitride compound semiconductor, comprising a film at least containing polycrystalline metal.

(105) FIG. 9 is a cross sectional structural view illustrating a seventh embodiment of a bipolar transistor according to the present invention. At first, structural features of the embodiment will be outlined, and then the manufacturing method will be explained.

(106) This embodiment has a structure in which a single crystal silicon/germanium layer 51 is disposed only to the openings of insulating films 12 and 21, and a base lead electrode 31 comprising polycrystal silicon and the single crystal silicon/germanium layer 51 are in contact with each other by way of an extrinsic base 52. Various constitutions explained for Embodiments 1 to 6 can be used for the single crystal silicon/germanium layer 51.

(112) An n-type collector layer 3 at a low concentration is epitaxially grown over the entire surface of the p-type silicon substrate 1 formed with a high concentration n-type buried layer 2, and a device isolation insulating film 11 comprising a silicon oxide film is formed. The device isolation is conducted by a usual method. Then, a collector/base isolation insulating layer 12 comprising a silicon oxide film, a collector/base isolation insulating film 21 comprising a silicon nitride film, a base lead electrode 31 comprising polycrystal silicon (or polycrystal silicon/germanium), and an emitter/base isolation

insulating film 13 are formed. Then, an opening of the emitter/base isolation insulating film 13 and the base lead electrode 31 is formed in the laminate structure by usual etching.

2. An electrode for p-type Group III nitride compound semiconductor according to claim 1,Washio et al. show wherein said polycrystalline metal has such a fiber structure that crystal planes of crystal grains are oriented.

3. An electrode for p-type Group III nitride compound semiconductor according to claim 2, Washio et al. show wherein said polycrystalline metal has large crystal grains.

Claims 1 to 3, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(b) as being anticipated by Ito et al. (U.S. Patent # 6770519 B2).

1. Ito et al (figures 1A to 9) specifically figure 1F show an electrode for p-type Group III nitride compound semiconductor, comprising a film at least containing polycrystalline metal.

[0033] As shown in FIG. 1E, boron (B.sup.+), which is a p-type impurity is ion implanted again using the sidewall spacers, which are made from the gate electrode 4, SiN film 7, and SiO.sub.2 film 8, as the ion implantation mask. The ion implantation conditions are, for example, acceleration energy of 5 keV and a dose amount of 3.times.10.sup.15 cm.sup.-2. With this ion implantation, deep impurity ion implantation regions 9 are formed in the surface layer of the silicon substrate 1 separated from the end of the gate electrode 4. In this case, a large amount of impurity ions B.sup.+ are also implanted in the gate electrode 4, which is made from polycrystal silicon.

2. An electrode for p-type Group III nitride compound semiconductor according to claim 1, Ito et al. show wherein said polycrystalline metal has such a fiber structure that crystal planes of crystal grains are oriented.

[0036] Typically, comparing an impurity implanted in polycrystal materials with an impurity implanted in single crystal materials, an impurity implanted in the polycrystalline materials diffuses easier at lower temperatures. This is because crystal grain boundaries, where an impurity easily diffuses, exist in the polycrystalline materials. Based on this

impurity diffusion characteristic, impurity in the polycrystal gate electrode may diffuse, but the diffusion of an impurity in the single crystal semiconductor substrate can be restricted, as in the above-mentioned pre-anneal temperature conditions. Boron implanted in the gate electrode 4, which is made from the polycrystal silicon, diffuses in the depth direction in accordance with the boron concentration gradient, and spreads around the entire layer of gate electrode 4 at a thickness of approximately 175 nm. On the other hand, boron implanted in the single crystal silicon substrate 1 has substantially no diffusion and stays in the ion implantation regions 9. In this way, it is possible to facilitate diffusion of only boron in the gate electrode 4 and keep a shallow junction depth without causing the diffusion of the boron impurity in the extension region 6 that has already been formed.

Detail Description Paragraph - DETX (19):
[0040] In this way, with the semiconductor manufacturing method according to this embodiment, the annealing process used for forming the source/drain region controls the diffusion of the impurity implanted in the single crystal silicon substrate 1. Also it is possible to both improve the transistor characteristics and form an extremely shallow junction of less than 20 nm since the annealing includes a pre-anneal (first heat treatment) and a flash-lamp annealing (second heat treatment). The pre-anneal (first heat treatment) is preformed under temperature conditions capable of facilitating the diffusion of impurity implanted in the gate electrode 4 made from the polycrystal silicon, and the flash-lamp annealing which is an extremely short-time annealing is performed under conditions capable of activating the impurity implanted in the single crystal silicon substrate 1.

3. An electrode for p-type Group III nitride compound semiconductor according to claim 2, Ito et al. show wherein said polycrystalline metal has large crystal grains.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/744,745	10/3/04
Other Documentation: foreign patents and literature in 257/744,745	10/3/04
Electronic data base(s): U.S. Patents EAST	10/3/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
10/3/04

Alexander O Williams
Primary Examiner
Art Unit 2826